INTEGRATED CIRCUIT DEVICES HAVING DATA INVERSION CIRCUITS THEREIN WITH MULTI-BIT PREFETCH STRUCTURES AND METHODS OF OPERATING SAME

Abstract of the Disclosure

Integrated circuit devices include data inversion circuits therein that are configured to evaluate at least first and second ordered groups of input data in parallel with an ordered group of output data previously generated by the data inversion circuit. The data inversion circuit is further configured to generate inverted versions of the first and second ordered groups of input data as versions of the first and second ordered groups of data in parallel at outputs thereof whenever a number of bit differences between the first ordered group of input data and the ordered group of output data is greater than one-half a size of the first ordered group of input data and a number of bit differences between the second ordered group of input data and the version of the first ordered group of input data is greater than one-half a size of the second ordered group of input data, respectively.